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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/841,775 | 04/24/2001 | Gregory J. Smith | 50019.45US01/P04877 | 6876 |

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| EXAMINER | |
|---|---|
| CHASE, SHELLY A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | 2 |

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/841,775 | SMITH, GREGORY J. | |
| | Examiner | Art Unit | |
| | Shelly A Chase | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-9 and 14-20* is/are allowed.

6)☒ Claim(s) *10-13,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1 to 22 are presented for examination.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **10** to **13** are rejected under 35 U.S.C. 102(e) as being anticipated by Sim et al. (USP 6546511 B1).

Claim **10**:

**Sim** teaches parallel testing of an integrated circuit including a plurality of functional blocks, the method comprising: a common input stimulus being applied to all the functional blocks (see col. 3, lines 25 to 30), interpreted as "creating a test to verify the redundancy of a functional block within a circuit," and a comparator receiving the outputs of each functional block, determining if the outputs are the same (see col. 3, lines 31 to 40), interpreted as "performing the test to verify the redundancy of the functional block within the circuit." Sim also teaches a discriminator checking the output of the functional block against a target signal to verify the test (see col. 3, lines 56 et seq.).

As per claim **11**, Sim teaches if the functional block passes the test the circuit is accepted (see col. 4, lines 1 to 13).

As per claim **12**, Sim teaches parallel testing of a plurality of functional blocks within the in the circuit (see col. 3, lines 22 to 25).

4. Claims **21** to **22** are rejected under 35 U.S.C. 102(b) as being anticipated by Liebergot et al. (USP 4233682).

Claim 21:

Liebergot teaches fault detection and isolation system for an integrated circuit wherein the integrated circuit includes a functional logic [10] and a duplicate functional logic [12] for testing multiple faults of the chip, the system comprising: fault detectors [21 & 23] receives the input data and control data that are routed to the logic chains [11 & 12] (see col. 3, lines 44 to 55), interpreted as "a means for accessing a plurality of

occurrences of the function on the circuit," comparators [41 and 44] receiving the outputs form the logic circuits and comparing the received outputs to detect for errors (see col. 4, lines 34 et seq.), interpreted as "a means for performing at least one test to verify the redundancy of the function on the circuit," and an error encoding circuit [27] receiving the compared output and determining if the chip should be isolated (see col. 5, lines 20 et seq.), interpreted as "a means for determining if the plurality of the occurrences of the function on the circuit passed the at least on test."

As per claim 22, Liebergot teaches an error handling chip for monitoring the testing of the chips and making a decision (see col. 5, lines 30 et seq.).

***Allowable Subject Matter***

5. Claims 1 to 9 and 14 to 20 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art made of record teaches a method and an apparatus for testing the redundancy of a circuit, for instance, Kim et al. (USP 4821271), discloses a method and circuit for checking integrated circuits including a functional redundancy checking logic wherein the output of the chip is checked within a certain time window and Johnson et al. (USP 4903270), teaches an apparatus for self-checking of functional redundancy check logic wherein a chip having identical modules is configure as a master and a checker and error detection is performed detecting errors in the checker. However, the prior art made of record taken alone or in combination fail to teach or fairly suggest or render obvious the novel elements of the instant invention.

Claims 1 and 14:

The prior art made of record fail to teach or fairly suggest an apparatus for verification of redundant functions on a circuit comprising: a test interface circuit including an input and an output arranged to receive an input signal, and in response to the input signal, supply a test signal, indicating a function on the circuit to test. Claims 2 to 5 and 15 to 20 are directly or indirectly dependent on claims 1 and 14 thus; these claims are allowable over the prior art made of record.

Claim 6:

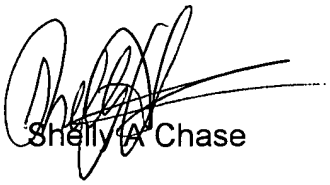
The prior art made of record fail to teach or fairly suggest an apparatus for redundant functions verification for an integrated circuit, the circuit a mixed signal circuit and configuration, control and testing circuitry for the mixed signal circuit, comprising: a protocol logic interface circuit arranged to receive a control signal and arranged to activate a test mode within the circuit in response to the control signal, the test mode arranged to test a functional block and a redundant functional block within the circuit. Claims 7 to 9 are directly or indirectly dependent on claim 6 thus; these claims are allowable over the prior art made of record.

## ***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A Chase whose telephone number is 703-308-7246. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Shelly A Chase